



Reissue
7/3-1804
v. Jones

PATENT
Attorney Docket No. 401191

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

HATAKENAKA et al.

Application No. 09/871,978

Art Unit: 2133

Filed: June 4, 2001

Examiner: D. Ton

For: SEMICONDUCTOR INTEGRATED
CIRCUIT DEVICE COMPRISING
RAM WITH COMMAND DECODE
SYSTEM AND LOGIC CIRCUIT
INTEGRATED INTO A SINGLE CHIP
AND TESTING METHOD OF THE
RAM WITH COMMAND DECODE
SYSTEM

REQUEST FOR CORRECTED OFFICIAL FILING RECEIPT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Several errors have been noted on the Official Filing Receipt in the referenced application. Applicants previously requested and received a corrected Filing Receipt for this patent application. However, the correction was incomplete. The patent, of which the present patent application is a reissue patent application, claimed no domestic priority and therefore all of the domestic priority data, which pertains to a different patent incorrectly listed on the original Filing Receipt, should be deleted. The patent of which reissue is sought claims the benefit of a foreign patent application and that priority claim information needs to be entered on the filing receipt under Foreign Applications. Please issue a Corrected Official Filing Receipt correcting this error as marked in red on the attached copy of the Official Filing Receipt.

In the portion of the Domestic Priority data as claimed by applicant, the portion that reads "WHICH IS A CIP OF 08/891,818 07/14/1997 ABN WHICH CLAIMS BENEFIT OF 60/021,829 07/16/1996 AND SAID 08/964,236 11/04/1997 CLAIMS BENEFIT OF 60/028,086 10/07/1996" is erroneous and should be removed.

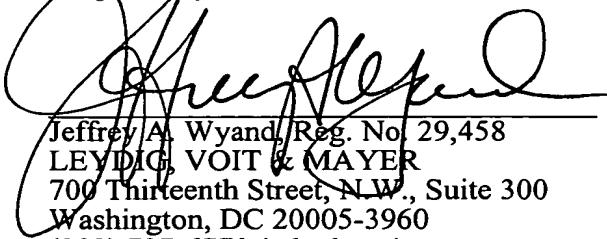
In re Appln. of Hatakenaka et al.
Serial No. 09/871,978

Under Foreign Applications please add JP 9-086600, filed April 4, 1997. These errors occurred at the U.S. Patent and Trademark Office.

A correct application data sheet is attached.

Prompt issuance of a completely corrected filing receipt is requested.

Respectfully submitted,



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Date: October 29, 2003
JAW:ves



UNITED STATES PATENT AND TRADEMARK OFFICE

COMMISSIONER FOR PATENTS
 UNITED STATES PATENT AND TRADEMARK OFFICE
 WASHINGTON, D.C. 20231
 www.uspto.gov

APPLICATION NUMBER	FILING DATE	GRP ART UNIT	FIL FEE REC'D	ATTY.DOCKET.NO	DRAWINGS	TOT CLAIMS	IND CLAIMS
09/871,978	06/04/2001	2133	870	401191	14	18	4

O I P E

OCT 29 2003

U.S. PATENT & TRADEMARK OFFICE 8625

23548
 LEYDIG VOIT & MAYER, LTD
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 WASHINGTON, DC 20005-3960

CONFIRMATION NO. 5265
 CORRECTED FILING RECEIPT


 OC00000007130997

Date Mailed: 11/28/2001

Receipt is acknowledged of this nonprovisional Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Customer Service Center. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).

Applicant(s)

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Domestic Priority data as claimed by applicant

THIS APPLICATION IS A REI OF 08/964,236 11/04/1997 PAT 5,910,181
 WHICH IS A CIP OF 08/891,818 07/14/1997 ABN
 WHICH CLAIMS BENEFIT OF 60/021,829 07/16/1996
 AND SAID 08/964,236 11/04/1997
 CLAIMS BENEFIT OF 60/028,086 10/07/1996

Foreign Applications

JP 9-086600, filed April 4, 1997
 If Required, Foreign Filing License Granted 07/16/2001

Projected Publication Date: Not Applicable

Non-Publication Request: No

Early Publication Request: No

Title

Semiconductor integrated circuit comprising synchronous DRAM core and logic circuit integrated into a single chip and method of testing the synchronous DRAM core

Preliminary Class

714

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Title 35, United States Code, Section 184
Title 37, Code of Federal Regulations, 5.11 & 5.15**

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